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PATENT
Attorney Reference No. 6319-56134

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re application of: Chang, Chin-Huang

Art Unit: 1765

Application No. 09/660,753

Filed: September 13, 2000

For: METHOD FOR REDUCING SIZE OF SEMICONDUCTOR UNIT IN PACKAGING PROCESS

Examiner: Vinh, Lan

Date: September 3, 2002

CERTIFICATE OF MAILING

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Stacey C. Slater, Esq.
Attorney for Applicant

TRANSMITTAL LETTER

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Enclosed is an Amendment After Final Rejection for the above application. The fee has been calculated as shown below.

CLAIMS AS AMENDED					
For	No. after amendment	No. paid for previously	Present Extra	Rate	Fee
Total Claims		- *	=	$18.00	$ 0.00
Indep. Claims		**	=	$84.00	$ 0.00
Mult. Dep. Claims Fee (if not previously paid)				$280.00	
One-month Extension of Time				$110.00	
Two-month Extension of Time				$400.00	
Three-month Extension of Time				$920.00	
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$0.00

* greater of twenty or number for which fee has been paid.
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☒ No additional fee is required.

SCS:ch 09/03/02 6319-56134

PATENT
Attorney Reference No. 6319-56134

☒ Please charge any fees that may be required in connection with filing this amendment and any extension of time, or credit any overpayment, to Deposit Account No. 02-4550. A copy of this sheet is enclosed.

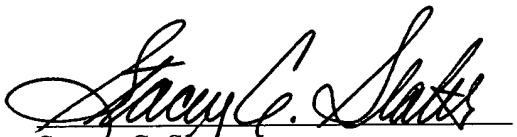
☒ Also enclosed are copies of 3 IEEE articles:

1. *Development of Tapeless Lead-On-Chip (LOC) Packaging Process with I-line Photosensitive Polyimide;*
2. *Polyimide Fatigue Induced Chip Surface Damage in DRAM's Lean-On-Chip (LOC) Packages; and*
3. *Effects of Mold Compound Properties on Lead-on-Chip (LOC) Package Reliability During IR Reflow.*

☒ Please return the enclosed postcard to confirm that the items listed above have been received.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By 

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#5 9/11/02

SCS:cb 09/03/02 6319-56134

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Response Under 37 C.F.R. § 1.116 Expedited Procedure

In re application of: Chang, Chin-Huang

Art Unit: 1765

Application No. 09/660,753

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Stacey C. Slater, Esq.
Attorney for Applicant

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AMENDMENT AFTER FINAL REJECTION

This responds to the Office Action (Final Rejection) dated July 03, 2002, concerning the application referenced above.

1. Claims 1, 2, 3, 5, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, and 20 were amended in applicant's communication filed May 13, 2002, in response to the first Office Action dated Feb 13, 2002.

2. The first Office Action dated Feb 13, 2002, was traversed in applicant's communication filed May 13, 2002 in response to the first Office Action dated Feb 13, 2002.

3. Applicant appreciates the Examiner's review of his response (filed May 13, 2002) to the first Office Action dated Feb 13, 2002, and respectfully requests reconsideration in light of the following remarks.

4. Reconsideration and allowance of amended claims 1, 2, 3, 5, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20 are respectfully requested in view of the following remarks. Original claims 4, 6, 7, and 8 ultimately depend on amended claim 1, and original claim 13 ultimately depends on amended claim 11, and for the reasons stated herein these claims are considered to be in condition for allowance.

Applicant respectfully traverses the Final Rejection alleging that claims 1-6, 8-11, 14-18 are unpatentable under 35 U.S.C. § 103(a) over Dery *et al.* (U.S. patent No. 6,074,895) in view of Hudak *et al.* (U.S. patent No. 5,656,552), claim 12 unpatentable under 35 U.S.C. § 103(a) over Dery *et al.* (U.S. patent No. 6,074,895) in view of Hudak *et al.* (U.S. patent No. 5,656,552) and further in view of Shimizu *et al.* (U.S. patent No. 6,355,569), claim 19 unpatentable under 35 U.S.C. § 103(a) over Siniaguine (U.S. patent No. 6,184,060) in view of Shimizu *et al.* (U.S. patent No. 6,355,569). Applicant also respectfully traverses the Examiner's response (Paragraph 8 of the Final Office Action) to applicant's arguments.

Regarding the Examiner's Final Rejection to amended claim 1, particularly lines 3-5 from the bottom of page 2 of the Final Office Action, please note that according to the art of Dery *et al.* (lines 23-55 of col 5, and Figs. 2A-2D) the passivation layer 211 or 111 (specifically the surface 211a or 111a thereof) of an IC chip (Figs. 2A-AD) instead of the second surface 210 of the IC chip is the part being modified by RIE (reactive ion etching). Lines 3-5 from the bottom of page 2 of the Final Office Action might have resulted from errors or the Examiner's misunderstanding. The surface identified as the second surface 210 of the IC chip in lines 3-5 from the bottom of page 2 of the Final Office Action, which is not the surface being etched but is the surface being back-to-back relative to the passivation layer 211 being etched according to the art of Dery *et al.*, corresponds to the second surface 23 (the surface being etched according to the present invention) of semiconductor unit 25 (Figs. 1-5). The surface 73 (the surface being etched according to the present invention) of semiconductor unit 75 (Fig. 7), as the second surface 210 of the IC chip in the art of Dery *et al.* and the second surfaces 23 / 73 of semiconductor unit in the present invention are all the surfaces being back-to-back relative to the surface with connection devices thereon. This can be seen from Figs. 2A-2D of Dery *et al.* where second surface 210 is back-to-back relative to surface 211a, which has connection devices 214 thereon, and from Figs 1-5 and Fig. 7 of the present invention where second surface 23 / 73 is back-to-back relative to surface 22 / 72, which has connection devices 24 (bumps) / 76 thereon. Although the numerical reference 210 is used by Dery *et al.* for referring to a chip according to lines 30-61, col. 5 of Dery *et al.*, while being used by the Examiner to refer to the second surface of a chip according to line 5 from the bottom of page 2 of the Final Office Action, the truth of the foregoing fact is not affected, i.e., the way of treating a semiconductor unit / chip by etching according to the present invention is substantially

different from the way according to the art of Dery *et al.* Related elaboration had been made in the second paragraph of page 4 of applicant's response (filed May 13, 2002) to the first Office Action.

Four significant differences between the present invention and the art of Dery *et al.* are described below.

The first difference is what has been mentioned above: the way of treating a semiconductor unit / chip by etching, i.e., the present invention etches the semiconductor unit / chip 25 from the second surface 23 (Figs. 2-4) or etches the semiconductor unit / chip 75 from the second surface 73 (Fig. 7 with reference to lines 14-21 of page 8), either the second surface 23 or 73 having no connection devices thereon and being back-to-back relative to the surface 22 (in Figs. 2-4) / 72 (Fig. 7), which have connection devices 24 / 76 thereon. In contrast, Dery *et al.* etches the surface 211a of passivation layer 211 (lines 55-57 of col 2, and lines 5-55 of col 5), which has connection devices 214 thereon and corresponds to the surface 22 or 72 of the present invention, the surface 22 or 72 being back-to-back relative to the second surface 23 or 73 according to the present invention (Figs. 1-5 and Fig. 7). The surface 23 or 73 etched according to the present invention is the one without connection devices thereon, while the surfaces 211 (or 211a) and 224 etched according to the art of Dery *et al.* are the ones with connection devices (214 and 226 in Figs. 2A-2D) thereon.

The second difference is that the etching according to the present invention performs a function of removing part of volume of a semiconductor unit / chip from the second surface thereof that has no connection devices thereon, while the etching according to the art of Dery *et al.* performs a function of modifying the structure of a surface (the surface with connection devices thereon, usually is a surface of a passivation layer) of a chip. The volume of a semiconductor unit / chip removed according to the present invention is an integration of a plurality of successive surfaces removed by etching the semiconductor unit / chip from the surface having no connection devices thereon, while the modified structure of the surface etched according to the art of Dery *et al.* is actually part of the etched surface itself, as can be understood from lines 6-34 of col 3 of the art of Dery *et al.* No matter how much the passivation layer is etched according to the art of Dery *et al.*, no thickness reduction of the entire chip (certainly includes its connection devices) can result because the locations of connection devices (either contact pads 212 or bumps 214) are independent of the thickness of the passivation layer 211. It can thus be seen the etching according to the present invention results in a thickness reduction of a semiconductor unit / chip, which is very significant and critical to the size and

packaging process of a semiconductor product. Etching according to Dery *et al.* has no effect that reduces a chip's thickness, i.e., the function and the result (or effect) of the etching according to the present invention is substantially different from those according to Dery *et al.*

Although the modification of a surface of a chip carrier by etching is not relevant to the size reduction of a chip by etching according to the present invention, applicant here makes comments on lines 57-58 and lines 13-14 of column 4 in the art of Dery *et al.* Lines 57-58 and lines 13-14 of column 4 in Dery *et al.* disclose using plasma 116 to remove some of the resin on the surface 124 of a chip carrier (not a chip / semiconductor unit), the result / effect of which is to expose filler thereon. Removing some of the resin on the surface 124 (of column 4) of a chip carrier does not and shall not have a size reduction effect for the chip carrier because the sizes and locations of the connection devices (contacts 126) on surface 124 are independent of the resin.

The third difference is that the object of the present invention is to reduce the size (thickness) of a semiconductor unit / chip, while the object of the art of Dery *et al.* is to enhance the adhesion between encapsulant and a chip and between encapsulant and a chip carrier, so that the incidence of delamination at the interfaces between the encapsulant and the chip and between the encapsulant and the chip carrier can be reduced. Related explanations had been made in the last line of page 4 and lines 1-4 of page 5 of applicant's response (filed May 13, 2002) to the first Office Action.

The fourth difference is the way of seating the object device being treated by etching. The object device treated by etching according to the present invention is a semiconductor unit / chip 25 seated on a chip carrier 21 (Figs. 2-4), while the object device treated by etching according to the art of Dery *et al.* is a chip 110 seated on an electrode 132 (Fig. 1A) or a chip carrier 120 seated on electrode 132 (Fig. 1C) or an integration of chip 210 and chip carrier 220 as a whole seated on electrode 232 (Fig. 2C). The object device treated by etching according to Fig. 2C in the art of Dery *et al.* is <u>not</u> a chip but are some portions (connection side surface 211a or 211 of the chip and some surfaces of the chip carrier) of a whole unit composed of a chip and a chip carrier (lines 33-55 of col 5), with electrode 232 as the seating apparatus for the whole unit. It can thus be seen that the object device treated by etching according to the present invention is seated on a chip carrier 21 (Figs. 2-4) which, after the etching is completed, is then packaged together with the object device to form a product; while the object device treated by etching according to the art of Dery *et al.* is seated on an electrode 232 (Fig. 2C), which is part of etching equipment, not part of the package product to be made.

In view of the above four differences between the present invention and the art of Dery

et al., it can be understood that the present invention differs from the art of Dery *et al.* in terms of way, function, result, and object of treating a semiconductor unit / chip by etching.

Explanations of the differences between the present invention and the art of Hudak *et al.* were made in the last paragraph of page 5 and the first two paragraphs of page 6 of applicant's response (filed May 13, 2002) to the first Office Action.

It can be seen from the above elaborations of differences between the present invention and the art of Dery *et al.*, and the explanations of differences between the present invention and the art of Hudak *et al.*, that it cannot be obvious to those of ordinary skill in the art to think of combining the arts of Dery *et al.* and Hudak *et al.* to provide the methods of claim 1 of the present invention, and to provide the advantages achieved by the present invention. Accordingly, the amended claim 1 overcomes the obviousness rejection based on Dery *et al.* and Hudak *et al.*

Regarding the Examiner's Final Rejection (lines 6-8 from the bottom of page 2, and lines 5-8 of page 4) to amended claims 9 and 11, please note that "lead-on-chip configuration" is a term publicly recognized in the field of IC package. What is shown in Figs. 2C and 2D of the art of Dery *et al.* with reference to lines 41-47 of col 5 is a flip chip configuration, not a lead-on-chip configuration. Many U.S. patents such as Nos. 5,572,066, 5,863,805, 6,025,212, and 6,183,589, may be referred to for information about lead-on-chip configuration. Three papers respectively characterizing 3 IEEE articles focusing on lead-on-chip configuration are enclosed herewith to show that the term "lead-on-chip" is publicly recognized in the field of IC package. A typical lead-on-chip configuration representing one aspect of the present invention is shown in Fig. 7 with reference to lines 20-24 of page 9. To applicant's best knowledge, no prior art has ever suggested etching for reducing the size of a chip when making a lead-on-chip package.

Regarding the Examiner's Final Rejection (lines 12-14 of page 4) to amended claims 15 and 16, please note that the lines 44-46 of col 5 of the art of Dery *et al.* do not mention using epoxy/adhesive material between the chip and the chip carrier. The epoxy resin mentioned in lines 14 of col 4 of the art of Dery *et al.* is a protective coating also used as solder mask and mainly used to control thermal expansion coefficients (lines 10-14 of col 3). The connection between the chip and the chip carrier according to the art of Dery *et al.* is a flip chip configuration, and the connection between the chip and the chip carrier is done completely via solder bumps 214 soldered to contact pads 212 of the chip and contact pads 226 of the chip carrier. Neither the passivation layer of a chip nor the epoxy resin on the surface of a chip carrier according to the art of Dery *et al.* functions as adhesive material to provide

adhesion between the chip and the chip carrier in the flip chip configuration. This is because a flip chip configuration is substantially different from other package configurations, such as a lead-on-chip configuration. To applicant's best knowledge, no prior art has ever suggested using adhesive material to provide adhesion between the chip and the chip carrier in a flip chip configuration. This is a reasonable result as a flip chip configuration is significantly different from the other package configurations, such as a lead-on-chip configuration.

Regarding the Examiner's Final Rejection (lines 15-17 of page 4) to amended claim 17, please note that (col 4, lines 11-12) of the art of Dery *et al.* do not disclose using laminate 122 to cover/shield chip carrier 120 either before or when performing etching, and it is actually irrelevant even if anything is used to cover/shield chip carrier 120 before etching. In fact, it is irrelevant to argue over using laminate 122 to cover/shield chip carrier 120, because a chip carrier is mainly composed of laminate intended for carrying a chip. It is unreasonable to cover/shield a chip carrier by its own main structure.

Regarding the Examiner's Final Rejection (lines 1-14 of page 5 and lines 9-20 of page 6) to amended claims 12 and 19, please note that Shimizu *et al.* neither disclose applying beams of light to a surface of an object device to etch the surface, nor suggest applying beams of light to a surface of an object device to reduce the size of the object device. The art of Shimizu *et al.* uses light beam 40 to control the velocity of neutral radicals reaching a surface of an object device 12.

Regarding the Examiner's response (the last paragraph of page 8 and the first paragraph of page 9 of Final Office Action) to applicant's argument filed May 13, 2002, please note that applicant has respectfully traversed it by relevant remarks above (please refer to explanations of the second difference between the present invention and the art of Dery *et al.*). It deserves further emphasis that removing part of volume (which is an integration of a plurality of successive surfaces) of an object device according to the present invention is substantially different from modifying (such as roughening) the structure of a surface of an object device according to the art of Dery *et al.*

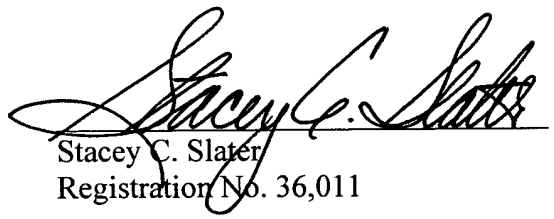
Regarding the Examiner's response (the second paragraph of page 9 of Final Office Action) to applicant's argument filed May 13, 2002, please note that applicant has respectfully traversed it by relevant remarks above (please refer to explanations of the fourth difference between the present invention and the art of Dery *et al.*). It deserves further emphasis that a seating apparatus is the apparatus for seating an object device to which an operation is applied. The object device to which an operation (etching) is applied according to the present invention is a semiconductor unit / chip, while the object device to which an operation (etching) is applied according to the art of Dery *et al.* is the

whole unit composed of a chip and a chip carrier. If the chip carrier in the art of Dery *et al.* is deemed a seating apparatus for the chip, then what is the seating apparatus for the chip carrier? Even if the chip carrier is seated on an ordinary table, the table is deemed a seating apparatus for the chip carrier. Please note the chip carrier in the art of Dery *et al.* is part of the object device. It can thus be understood that the electrode 232 in the art of Dery *et al.* is actually the seating apparatus for the object device.

Accordingly, the amended claims 1, 11, and 19 overcome the obviousness rejection based on Dery *et al.*, Hudak *et al.*, Siniaguine, and Shimizu, and are in condition for allowance and such actions are respectfully requested. Claims 2-10 depend on the amended claim 1, claims 12-18 depend on the amended claim 11, and claim 20 depends on the amended claim 19, all are therefore in condition for allowance and such actions are also respectfully requested.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By 

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Development of Tapeless Lead-On-Chip (LOC) Packaging Process with I-line Photosensitive Polyimide

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ABSTRACT

A double-sided adhesive tape is typically used as an insulator and mechanical buffer layer between the chip and lead frame in lead-on-chip (LOC) packages. The costs associated with the lead frame and tape process make the current LOC package more expensive than conventional packaging. A new tapeless LOC package process has been developed which significantly reduces the production costs. In this new process, the tape is replaced by a I-line photosensitive thermosetting polyimide layer coated on the passivation deposited wafer. This paper describes the optimum material properties for the polyimide, the fabrication process parameters, and the experimental and simulated reliability and performance results of the tapeless LOC package.

I. INTRODUCTION

The dramatic increase in the number of devices and functionality of the latest ultra large scale integration (ULSI) designs have resulted in increasing chip size. Concurrently, to achieve higher circuit board component densities, package dimensions have been shrinking. These two competing trends are leading to ever more rigorous requirements on the thermal and mechanical characteristics of the packaging technology. Furthermore, the demand for increased device functionality naturally leads to smaller feature sizes which are often more sensitive to package-induced stress. The LOC package [1-3] has begun to replace conventional package designs since it offers more margin from the chip or die pad edge to the package outline. In the LOC packaging technology, the lead fingers are attached directly to the surface of polyimide deposited on the chip using a double-side adhesive tape. Polyimide films are currently being used as stress buffers and adhesion promoters, to protect circuit elements from package-induced stress damage and to avoid catastrophic corrosion-related failures. While the LOC package offers clear advantages over conventional package designs, its cost is significantly higher due to the added complexity of the lead frame and double-side adhesive tape. In an effort to reduce production cost, a tapeless LOC packaging technology has been developed. As its name implies, the tapeless LOC design removes

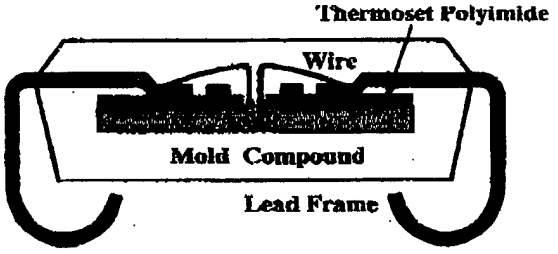

Figure 1 Small outline J-lead (SOJ) package with tapeless LOC design.

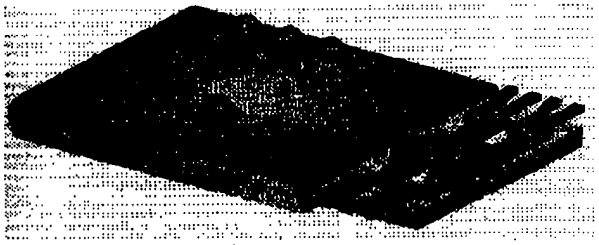

Figure 2 Chip scale package (CSP) with tapeless LOC design.

Effects of Mold Compound Properties on Lead-on-Chip (LOC) Package Reliability During IR Reflow

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ABSTRACT

This paper reports the investigation into Lead-On-Chip (LOC) package cracking resistance, the effects of mold compound properties, and the package cracking predication. The vehicle for such investigation was a DRAM LOC package and four mold compounds under two IR reflow processes (220°C and 260°C).

As the reliability of the LOC package is strongly dependent on the mechanical properties of the mold compound, great efforts were put into its characterizations. The mold compound characterization was conducted using an Instron Universal Tester with a temperature chamber which regulated the testing temperature from -60 to 260°C. These characterizations included temperature dependence, loading speed effects, moisture effects, creep behavior, etc..

The linear elastic fracture mechanics method was used to predict package cracking resistance. This included obtaining mold compound fracture toughness through 3-point bending test at the IR reflow temperatures, finite element analysis to obtain package stress intensity factors at these conditions, and correlate with the package reliability test results.

INTRODUCTION

Moisture-induced package cracking mechanism and criteria during solder reflow for conventional chip-on-pad packages have been extensively investigated. While the lead-on-chip (LOC) package has some similar failure phenomena during solder reflow, it has its own unique failure mechanism. In the LOC packaging technology, the lead fingers are attached directly to the surface of polyimide deposited on the chip using a double-sided adhesive tape, and there is no chip pad. The failure mechanism for the LOC package has been explained as high internal stresses develop when the package is exposed to temperatures different from the molding temperature due to the mismatch in the coefficients of thermal expansion (CTE) among the materials within the package. The steam pressure created by vaporization of absorbed moisture in the mold compound and the LOC tape during reflow soldering adds to much higher internal stresses. As a result, the mechanical tolerance of the package can be exceeded, leading to delamination at the LOC tape and subsequently mold compound crack initiation at the LOC tape corner and crack propagation in the mold compound. Figure 1 shows a typical LOC package failure after IR reflow, where the delamination at the LOC tape/die interface can be clearly seen. The mold compound crack initiated at the tape corner at an angle of about 10° to the interface.

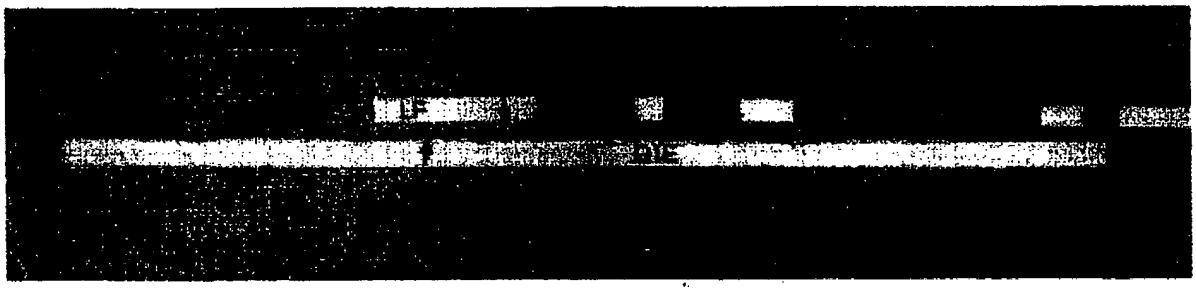

Figure 1. Delamination and Mold Compound Fracture after IR Reflow

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Polyimide Fatigue Induced Chip Surface Damage in DRAM's Lead-On-Chip (LOC) Packages

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Abstract - The effect of mechanical fatigue on reliability failure was studied, based on plastic fracture mechanics including stress intensity factor, stress singularity, micro-plastic deformation behavior, and stress-strain characteristics. The fatigue has made the mechanical stability of novel lead-on-chip (LOC) packaging technologies a grave concern. The dominant issue is device failure related to fracture in the passivation layers and Al-Si-Cu metal due to polyimide cracking caused by fatigue in temperature cycles. To investigate the effect of polyimide fatigue on chip surface damage, devices were fabricated with different types of polyimides. A fatigue model obtained from the experiment and the simulated results of plastic deformation behavior were discussed. The validity of the proposed fatigue model was verified by experiments on different types of epoxy molding compounds. The results of these characterizations and an explanation of the primary factors affecting polyimide fatigue are presented in this paper.

I. INTRODUCTION

The dramatic increase in the number of devices and functionality of the latest ultra large scale integration (ULSI) designs have resulted in increasing chip size. Concurrently, to achieve higher circuit board component densities, package dimensions have been shrinking. These two competing trends are leading to ever more rigorous requirements on the thermal and mechanical characteristics of the packaging technology. Furthermore, the demand for increased device functionality naturally leads to smaller feature sizes which are often more sensitive to package-induced stress. As a result of these demands, the LOC package [1-6] (shown in figure 1) has begun to replace conventional package designs since it offers more margin from the chip or die pad edge to the package outline. In the LOC packaging technology, the lead fingers are attached directly to the surface of polyimide deposited on the chip using a double-side adhesive tape. Polyimide films [7-11] are currently being used as stress buffers and adhesion promoters, to protect circuit elements from package-induced stress damage and to avoid catastrophic corrosion-related failures. After a high temperature chip mounting process, the adhesive tape shrinks during cool down to room temperature and subsequent to temperature cycling tests. This stress potentially causes a heavily damaged polyimide surface. This damage in turn leads to crack formation in the polyimide, and eventually to fracture in conjunction with the passivation layers and Al-Si-Cu metal. An example of the polyimide cracking induced by interfacial delamination between the epoxy molding compound and the tape is illustrated in figure 2. This result is typical of the loss of polyimide fatigue strength during temperature cycles. The effect of material composition on chip surface damage and its temperature cycle performance have been previously considered [9-11]. The effect of assembly process parameters relevant to the damage has also been studied [12-14]. These methods have demonstrated vastly improved polyimide cracking resistance but contained no explanation of polyimide fatigue caused by interfacial delamination between the polyimide and the epoxy molding resin.

This paper describes a fatigue model to predict the useful life of polyimides associated with the accumulated damage during temperature cycles. The model showing polyimide fatigue was obtained from the stress intensity factor, stress singularity, polyimide stress-strain characteristics and plastic deformation behavior. The magnitudes of stress obtained by finite element method (FEM) analysis were used to calculate the stress intensity factor in resolving a stress singularity and subsequently to define the values of polyimide plastic strains. A tensile test was carried out to determine polyimide stress-strain characteristics. The validity of the proposed model was verified by experiments on seven types of molding compounds affecting different magnitudes of polyimide strains.

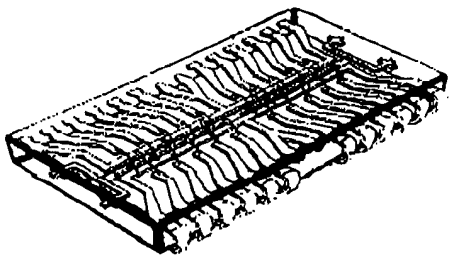

Figure 1 Small-outline-J-lead (SOJ) package with LOC design.

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